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Exploring Diverse Approaches in VLSI Design Methodologies

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ABSTRACT: The field of Very-Large-Scale Integration (VLSI) design has witnessed significant evolution, driven by advances in technology and the increasing complexity of integrated circuits. This paper provides a comprehensive examination of various methodologies employed in VLSI design, aiming to shed light on their unique advantages, limitations, and applications. We categorize the methodologies into traditional, contemporary, and emerging approaches, including Full Custom Design, Standard Cell Design, and ASIC/FPGA-based design strategies. Through comparative analysis, we explore how each approach addresses key design challenges such as scalability, power efficiency, and design flexibility. The paper also discusses the impact of automated tools and software innovations on the efficiency of VLSI design processes. By highlighting case studies and practical examples, we illustrate the effectiveness of these methodologies in real-world scenarios. This study serves as a valuable resource for both practitioners and researchers, offering insights into selecting the most suitable VLSI methodology based on specific project requirements and constraints.

KEYWORDS: Dynamic Power, Leakage power, Very Large - Scale Integrated (VLSI), VLSI design.

I. INTRODUCTION

VLSI layout is divided into 2 types: high wattage VLSI layout and lower power consumption VLSI design[1][2]. This paper will discuss the recent advancements and trends in reduced power VLSI design[4][5] The purpose of this essay is also to illustrate and prove the present and future trends in low power VLSI research and development. [6].In the field of electronics, the breadth of VLSI is also fairly broad[7].

Between numerous different papers within the subject of VLSI study as well as VLSI design technique, a document entitled presents a notion of a way of reduced power VLSI[8]. Also, several approaches were employed to tackle complicated complex challenges of computer system as well as electronics systems[3]. The Layout of VLSI Design Methods by Lynn Conway discussed the origins of VLSI, stating that in the early 1970s, a British scientist named Carver Mead began a research and study series titled electronic circuit design, in which he mentioned how very large scale work could be done with the help of small chips, and during this time he founded the nMOS design industry[9][10]. The circuit architecture and physical design of a VLSI design are shown in Figure 1[11].

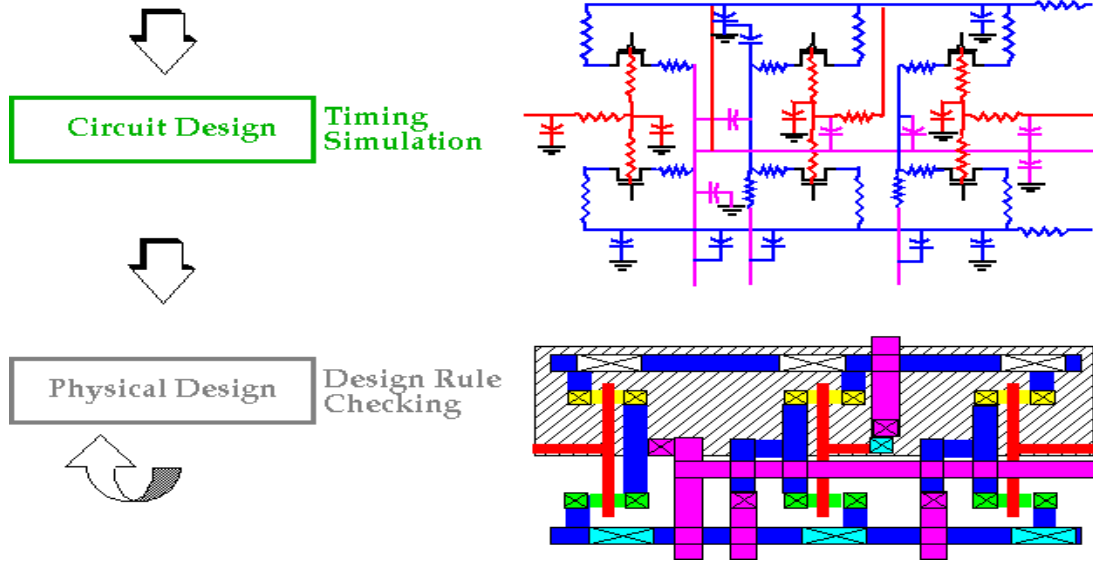


Figure1: Illustrating the Principle of VLSI Design

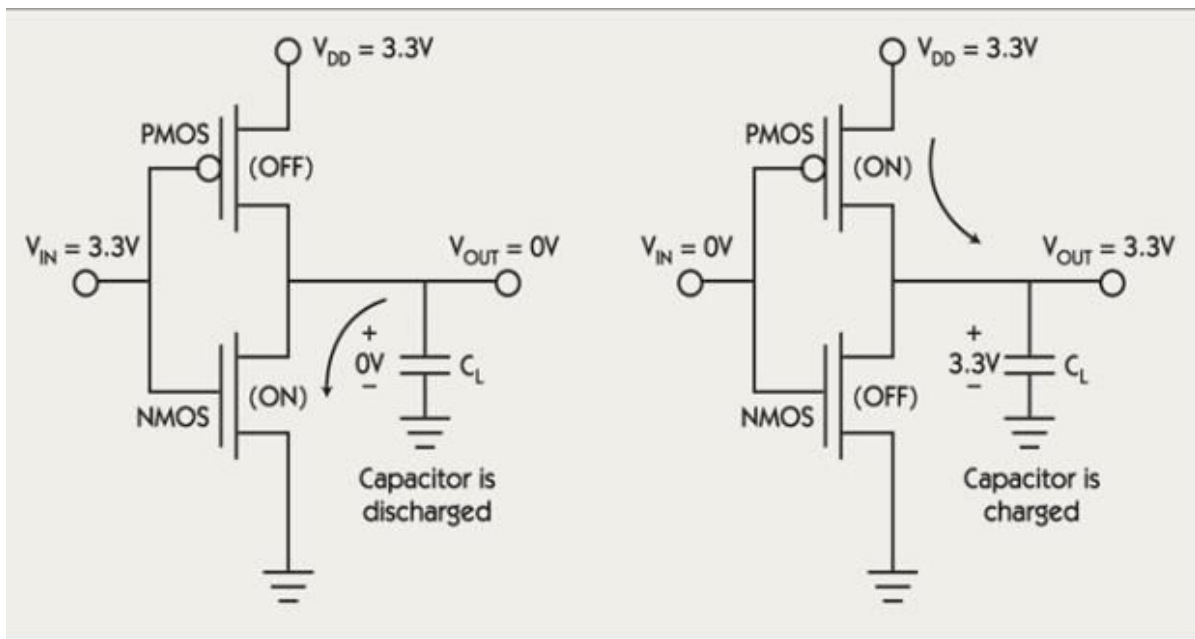


Figure2: Illustrating the Reduction of Dynamic Power

A. Dynamic Power

Dynamic power is the energy consumed by a system as a device switches from one state to another, and this activity may be seen using VLSI design.[12][13]. The power utilized when the device is charging the loads connected to the item, as well as the fault current power of the device when it is charging, is referred to as dynamic power. The power dissipation that can occur in CMOS is seen in Figure 2 [14][15].

B. Leakage Power

Leakage power of VLSI hardware, where a certain amount of waste power is not used by the scheme once the scheme switches from one state to the other, leakage electricity generated by the system when the device is not linked to transitions, and then when the gadget is both static as well as trying to switch, but the most important issue associated with leakage power is when the gadget has been in an inactive form.[16][17].



II. LITERATUREREVIEW

There have been numerous publications in field of VLSI, because it is a rapidly growing and very well technology in the field of computers. There have been numerous applications of VLSI in various fields, including computer systems, cellular telephones, and transistor chip resizing. Various methodologies were also used to resolve complex issues of embedded scheme and electronic parts processes [21].

In this article, a graphic titled "Knowledge Dissemination and Evolution" was shown, which discussed how different techniques practitioners developed into practise artefacts. The many types of CMOS and nMOS were discussed by a receiving community. The MPC experiences sketched out how the experiment approach and computer connection architecture were implemented [18].

This page include satable displaying the diverse structure and result so fVLSI design, as well as the numerous Out comes based on the Joint Evolution of the Multi-Level Cluster of Systems. Different work and research in the subject of VLSI design, as well as current work in knowledge engineering, have been discussed (19). Due to its complexity, VLSI design maybe challenging to solve, and societal considerations, infrastructure, and scale impact can all affect VLSI design techniques. Finally, in the sphere of extremely large-scale integration, provide knowledge engineering that allows knowledge transformation [4] [25].

L. A. Hemaspaandra addressed the necessity for VLSI in electronic domains like computer systems, mobile phones, semiconductors, and so on in research papers (19). The dynamic powers of electronic circuit is swallowed by the device when the gadget is extremely freely and readily transformed or flowing from one state to another, according to this study [20] [22]

However, the most popular and mainstream approaches include clock gating, which is a highly effective way for reducing leakage power into the loop and also indicates that the modification of threshold voltage is precisely proportional to the delay and leakage current in a graphical representation. Clustered voltage scaling is the second most common technique for reducing leakage power [23] [24].

III. DISCUSSION

Low power and High power VLSI design are the two types of VLSI design. This paper will look at current developments and trends in reduced VLSI design. Low power VLSI is fixed area, according to the results, since it is responsible about everything from the transistor sizing to process shrinkage, voltages scaling, clock gating, and adiabatic logics. The goal of that research is to show and prove existing and future trends and developments in the field of low-power VLSI. In the field of electronics. In the field of electronics, the breadth of VLSI is also fairly broad [7]. Between numerous different papers with in the subject of VLSI study as well as VLSI design technique, a document entitled presents a notion of a way of reduced power VLSI [8]. Also, several approaches were employed to tackle complicated complex challenges of computer system as well as electronics systems

IV. CONCLUSION

This article also exhibits current and new improving technologies in field of the VLSI methodology and design, which is based on the research and design of VLSI. To fully comprehend the Mead-Conway approach, first learn about the specific idea, which explain show the qualities of certain knowledge systems, techniques, and substructure impact extents and rates of, diffusion, creation, convergence, knowledge, integration, and displacement. Many topics of the VLSI design approach are explained and clarified. This article presents thoughts and research on key cognitive and social phenomena that occur through out the theory creation, testing, and theory revision processes that are involved in the design of design knowledge. We have gained the confidence and understanding to dig more thoroughly into the qualities of knowledge and the processes of its evolution as a result of this effort. As a result, we are identifying potential for the practical application of computer science and artificial intelligence findings to the creation and deployment of new knowledge engineering concepts.

VLSI has wide ranges of the applications in field of electronics. A document named provides a thought of a means of reduced power VLSI is among a number of articles on the subject of VLSI research and design approach. In addition, numerous ways were used to address the complex issues of computer and electronics systems. The origins of VLSI were discussed in Lynn Conway's The Layout of the VLSI Design Methods, that stated that in early 1970s, a British scientist name Carver Pear brandy began a study and research series titled electronic circuit designs, in which he



mentioned how large scales work could done by help of small chips, and during this time he founded the nMOS design industry.

REFERENCES

1. Sharma M, Gupta N, Gupta R. POWER REDUCTION TECHNIQUES IN VLSI. *Int J Eng Technol Manag Res.* 2020;
2. Soumya N, Sai Kumar K, Raghava Rao K, Rooban S, Sampath Kuma R P, Santhosh Kumar GN. 4-bit multiplier design using cmos gates in electric VLSI. *Int J Recent Technol Eng.* 2019;
3. Liu B, Qu G. VLSI supply chain security risks and mitigation techniques: A survey. *Integr VLSI J.* 2016;
4. Brown RB, Bernhardt B, LaMacchia M, Abrokwah J, Parakh PN, Basso TD, et al. Overview of complementary GaAs technology for high-speed VLSI circuits. *IEEE Transactions on Very Large Scale Integration (VLSI) Systems.* 1998.
5. Kumar SBV, Rao P V., Sharath HA, Sachin BM, Ravi US, Monica B V. Review on VLSI design using optimization and self-adaptive particle swarm optimization. *Journal of King Saud University-Computer and Information Sciences.* 2020.
6. Sub-threshold Design for Ultra Low-Power Systems. *Sub-threshold Design for Ultra Low-Power Systems.* 2007.
7. Zhang Y. A foundation for the design and analysis of robotic systems and behaviors. *ProQuest Dissertations and Theses.* 1994.
8. Venkatraman S, Sundhararajan M. Area and interconnect length optimization for VLSI floor planning problem by using harmony search algorithm. *Int J Recent Technol Eng.* 2019;
9. Tsunekawa Y, Hinosugi M, Miura M. Design and VLSI evaluation of a high-speed cellular array divider with a selection function. *Electr Eng Japan (English Transl Denki Gakkai Ronbunshi).* 1998;
10. Saab Y. New 2-way multi-level partitioning algorithm. *VLSI Des.* 2000;
11. Ignatyev V V., Kovalev A V., Spiridonov OB, Kureychik VM, Ignatyeva AS, Safronenkova IB. Hybrid genetic-paired-permutation algorithm for improved VLSI placement. *ETRI J.* 2021;
12. Scalise F, Balanza M, Chauve N, Combelles P, Penard P, Del Toso C, et al. A prototype VLSI solution for digital terrestrial TV receivers conforming to the DVB-T standard. *SMPTE J.* 1997;
13. Venkatraman S, Sundhararajan M. A metaheuristic algorithm for VLSI floorplanning problem. *Int J Recent Technol Eng.* 2019;
14. Scalise F, Balanza M, Chauve N, Combelles P, Penard P, Del Toso C, et al. A Prototype VLSI Solution for Digital Terrestrial TV Receivers Conforming to the DVB-T Standard. In: *International Workshop on HDTV 1996.* 2015.
15. Chen X, Liu G, Xiong N, Su Y, Chen G. A Survey of Swarm Intelligence Techniques in VLSI Routing Problems. *IEEE Access.* 2020;
16. Wolf M, Mukhopadhyay S. VLSI for the Internet of Things. *Computer (Long Beach Calif).* 2017;
17. Sravani MM, Ananiah Durai S. Attacks on cryptosystems implemented via VLSI: A review. *J Inf Secur Appl.* 2021;
18. Macii E, Pedram M, Somenzi F. High-level power modeling, estimation, and optimization. *IEEE Trans Comput Des Integr Circuits Syst.* 1998;
19. Sakemi Y, Morino K, Morie T, Aihara K. A Supervised Learning Algorithm for Multilayer Spiking Neural Networks Based on Temporal Coding Toward Energy-Efficient VLSI Processor Design. *IEEE Trans Neural Networks Learn Syst.* 2021;
20. Hemaspaandra LA. SIGACT news complexity theory column 31. *ACM SIGACT News.* 2001;
21. Sathasivam S, Mamat M, Mansor MA, Kasihmuddin MSM. Hybrid discrete hopfield neural network based modified clonal selection algorithm for VLSI circuit verification. *Pertanika J Sci Technol.* 2020;
22. Dewan MI, Kim DH. NP-Separate: A New VLSI Design Methodology for Area, Power, and Performance Optimization. *IEEE Trans Comput Des Integr Circuits Syst.* 2020;
23. Bartolozzi C, Indiveri G. Synaptic dynamics in analog VLSI. *Neural Comput.* 2007;
24. Sivakumar R, Jothi D. Recent Trends in Low Power VLSI Design. *Int J Comput Electr Eng.* 2014;6(6):509–23.
25. Elrabaa MS, Abu-Khater IS, Elmasry MI, Elrabaa MS, Abu-Khater IS, Elmasry MI. Low-Power VLSI Design. In: *Advanced Low-Power Digital Circuit Techniques.* 1997.



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