e-ISSN:2582-7219

INTERNATIONAL JOURNAL OF MULTIDISCIPLINARY RESEARCH IN SCIENCE, ENGINEERING AND TECHNOLOGY

Volume 7, Issue 3, March 2024

INTERNATIONAL STANDARD SERIAL NUMBER INDIA

Impact Factor: 7.521

International Journal Of Multidisciplinary Research In Science, Engineering and Technology (IJMRSET)

| ISSN: 2582-7219 | www.ijmrset.com | Impact Factor: 7.521| Monthly Peer Reviewed & Referred Journal |

| Volume 7, Issue 3, March 2024 |

| DOI:10.15680/IJMRSET.2024.0703083 |

Performance Analysis of Fin FET based 6T & 8T SRAM Cell

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ABSTRACT: SRAM cell using FinFET technology to reduce power consumption. The proposed cell uses a 6T architecture with FinFET transistors in place of traditional CMOS transistors. Simulation results show that the FinFET-based SRAM cell has significantly lower leakage current and dynamic power consumption compared to the CMOS-based SRAM cell. The proposed design also achieves a high write margin, read stability, and read speed, making it suitable for low power applications in mobile and IoT devices. The results demonstrate that the FinFET-based SRAM cell provides a promising solution for reducing power consumption and improving performance in modern electronic systems.

KEYWORDS: FinFET, Dynamic Power, Low-power, SRAM,

I. INTRODUCTION

With increasing demand for the portable devices, the power consumption has become major concern for the VLSI chip designing. Technology scaling results in a significant increase in leakage current of CMOS devices which increases Power consumption of the device. As the integration density of transistors increases, leakage current which increases Power dissipation has become a major concern in today's designs. Considerable attention has been paid to the design of low power and high-performance SRAMs as they are critical components in both handheld devices and high-performance processors. Voltage scaling is fundamental to achieving energy efficient operation in digital circuits due to quadratic reduction in dynamic energy. SRAMs consume very much less energy than DRAMs and thus is an automatic choice over the latter. As SRAM does not require a refresh cycle because Data do not "Leak Away" Area of the design is a major concern for the SRAMs, as it is truly considered to be using more area of the silicon chip. The memory array is generally large, like for stand-alone SRAMs, the array covers as much as 60-70% of the total area of a chip, and for high-end embedded SRAMs it is about 50%.

As traditional planar CMOS technology seems to have reached its limits: increasing production costs are one of the main reasons preventing the move to the next technology node. One of the most promising substitutes for planar CMOS devices are FinFET-based architectures. Compared to their planar counterparts FinFETs provide improved gate control and near ideal sub- threshold swings that drastically lower leakage current. One of the key differences of FinFET transistors compared to planar MOSFETs is the width discretization. For FinFET-based designs the sizing is performed only by changing the number of fins.

There has been active research in recent years to analyse the impact of width quantization on SRAM performance and to evaluate reliability challenges of FinFET technology. The performance degradation of FinFET-based standard cells due to process variations has been evaluated. The impact of random and systematic variations on FinFET-based SRAM failure rates has been studied and design trade-offs in the presence of process variations have been examined on an SRAM cell with minimum sized transistors. To increase reliability of FinFET-based SRAMs against soft errors, two alternative methods have been suggested: increasing the number of fins of the transistors composing the cross-coupled inverters with significant area penalties, or by increasing the fin height. The impact of aging effects on FinFET-based SRAMs has been analysed.

FinFET technology is a type of 3D transistor design that has become increasingly popular in modern integrated circuit (IC) design. FinFET-based SRAM cells offer several advantages over traditional planar transistors, including improved performance and lower power consumption. The basic structure of a FinFET transistor involves a thin, vertical "fin" that is surrounded by a gate on three sides. This design allows for better control over the flow of electrons through the transistor, resulting in faster switching speeds and lower power consumption.

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In the context of SRAM cells, FinFET technology allows for higher density memory cells to be created, as the vertical design allows for more transistors to be packed into a smaller area. This results in higher capacity SRAM cells that can store more data, while also consuming less power. FinFET-based SRAM cells also exhibit better stability and reliability compared to planar transistors, as the 3D design helps to reduce issues such as gate leakage and short channel effects. This makes FinFET-based SRAM cells ideal for use in high-performance applications that require both high density and high reliability.

Overall, FinFET technology is a promising development in the field of IC design, offering significant benefits in terms of performance, power consumption, and reliability. It is expected to become increasingly popular in the design of future SRAM cells and other advanced ICs. Low Power FinFET-based SRAM cells are a type of memory cell that is designed to operate with minimal power consumption, making them ideal for use in battery-powered and portable devices. These memory cells incorporate FinFET transistor technology, which allows for improved performance and reduced power consumption compared to traditional planar transistors.

FinFET SRAM

In a Low Power FinFET-based SRAM cell, power consumption is minimized through the use of various design techniques, such as power gating, dynamic voltage and frequency scaling, and reduced supply voltage. Power gating involves selectively turning off sections of the circuitry that are not in use, effectively reducing their power consumption to zero. Dynamic voltage and frequency scaling involves adjusting the voltage and clock frequency of the memory cell based on the current workload, allowing for further power savings. Reduced supply voltage involves operating the memory cell at a lower voltage level, which reduces power consumption but can also impact performance.

Overall, Low Power FinFET-based SRAM cells offer significant benefits in terms of power consumption, performance, and reliability. They are ideal for use in applications that require high-density, low-power memory, such as portable devices, IoT devices, and wireless sensors. As the demand for low-power, high-performance devices continue to grow, the use of Low Power FinFET-based SRAM cells is expected to become increasingly popular in the design of future ICs.

The relentless scaling of semiconductor technology has resulted in dramatic performance improvements of Integrated Circuits (ICs). However, traditional planar CMOS technology seems to have reached its limit. To continue with Moore's law, FinFET technology has shown to be a viable solution. Process variations are still relevant, however. Therefore, it is crucial to study their impact on circuit performance. This paper explores design choices for 20nm FinFET-based SRAM cells and analyses the impact of process variations on the performance characteristics of the SRAM cell [4]. Power gating is commonly used to reduce leakage current in SRAM memories; leakage current has a large impact on SRAM energy consumption. We first focus on power gating FinFET SRAMs and then evaluate three techniques to reduce the leakage power and energy-delay product (EDP) of six- and eight-transistor (6T, 8T) FinFET SRAM cells. We compare the EDP savings obtained using: 1) power gating FinFETs; 2) near-threshold operation at VDD = 0.6 V instead of the nominal VDD = 1 V; and 3) alternative SRAM cells with shorted gate (SG) and low power (LP) configured FinFETs; LP-configuration reverse-biases a FinFET's back gate and reduces leakage current by up to 97%. SRAM cells with higher leakage benefit the most from power gating since they see the largest reductions in leakage current. Sharing power gating transistors among multiple SRAM cells can lead to more leakage current savings, but causes slower read and write speeds which can diminish their effectiveness. Alternative SRAM cells with lower leakage benefit the most from near-threshold operation to further reduce leakage current. Near-threshold operation and/or power gating reduces the 6T SG FinFET SRAM scheme's EDP slightly more than using the 8T SG FinFET SRAM scheme, but using an LP 8T SRAM scheme, such as LP_INV1.2, with near-threshold operation is more effective than power gating and provides the largest reductions in EDP. The design techniques recommended by this brief can enable longer battery life for small sensor systems and thus greater reliability for Internet-of-Things (IoT) devices [5]. For ultra-low-power applications, the computing components are smaller in size and consume less energy. In nonstationary signal analysis, the transformation plays an important role. Out of different transformation techniques, the most famous and dominant architecture is the discrete wavelet transforms. The building block of the architecture should be optimized by all parameters. In this paper, the optimization was done on the power reduction and leakage current reduction. A new FinFET-based lifting-based wavelet architecture was proposed. Power gating and reversible logic methodology are proposed for the FinFET-based transform to reduce the dynamic power by about 30%. The proposed FinFET-based processing elements were utilized in the various blocks of the lifting-based DWT architecture. The implementation was done in 32-nm CMOS and FinFET technology. From the results, it has been investigated that the FinFET-based circuits are efficient when compared with CMOS technology. This is due to the second-order effects

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happening in CMOS circuits below 45 nm. The proposed design consumes less area and low leakage current and power when compared with the CMOS technology [6].

The proposed finfet based 6t sram cell offers better stability in terms of static noise margin (snm) and read noise margin (rnm). During the read operations, sram cell stability analysis is based on the snm because many memory errors may occur. Since snm changes with each cell operation, a complete analysis of snm in read mode is required. In this paper, we look into the sram cell snm during read mode analysing various options to improve cell stability. These techniques are based on the transistor width, word-line, bit-line and supply voltage modulations. We show that it is possible to improve the stability of sram cell during read operations, while reducing word-line. To assess the efficiency of the approach, SPICE simulations in 45nm and 32nm FinFET technologies are used. The results show considerable improvements in terms of the standby power as well as the hold and read SNM. This suggests that the Vt-control method may be used for realizing low-standby power and robust SRAM [10].voltage which reduces the leakage current. We also analyse the temperature effect on snm, leakage current and leakage power for finfet based sram cell [9]. SRAM cell design methods for FinFET technology are proposed. One of the most important features of FinFET is that the independent front and back gate can be biased differently to control the current and the device threshold voltage. By controlling the back gate of FinFET, SRAM cell can be designed for minimum power consumption. This paper proposes a new 8T (8 transistors) SRAM structure that reduces dynamic power in writing operation and provides wider SNM (Static Noise Margin). Using the new FinFET based 8T SRAM cell, dynamic power consumption is reduced about 48% and the SNM is widened up to 56% compared to the conventional 6T SRAM at the expense of 2% leakage power and 3% write delay increase [11].

SRAM using Power Gating

FinFET-based SRAMs are widely used in modern electronic devices due to their superior performance characteristics, but they also consume significant power. To address this issue, several techniques have been developed to reduce the power consumption of FinFET-based SRAMs. One of the primary techniques is Power Gating, which involves turning off the supply voltage to a part of the circuit when it is not required. This technique is used to reduce leakage power in idle periods of the SRAM cell. Another approach is to use Multi -Vt Design, which involves using different threshold voltages for different transistors in the SRAM cell. This technique is used to reduce leakage power in the standby mode by using high Vt transistors in the standby mode and low Vt transistors during active mode. Body Biasing is another technique used to improve the performance of the SRAM cell at low supply voltages. It involves applying a voltage to the body of the transistor to adjust its threshold voltage. Voltage Scaling is a technique that involves reducing the supply voltage of the SRAM cell to reduce power consumption. This technique is used to reduce the dynamic power consumption of the SRAM cell.

Other techniques include Data-Dependent Power Management, Reducing the size of the SRAM cell, Write-Assist Techniques, Sense Amplifier Design, Low-power cache hierarchies, and Sleep Transistors. By using a combination of these techniques, power consumption in FinFET-based SRAM cells can be significantly reduced, resulting in longer battery life and more energy-efficient microprocessors. Power gating is a technique used to reduce power consumption in integrated circuits by

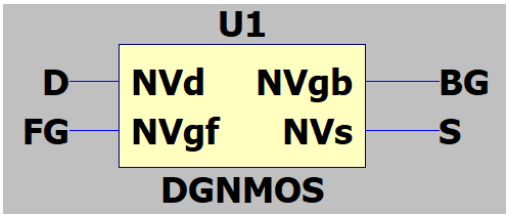

Figure 1: N-FinFET Sub circuit

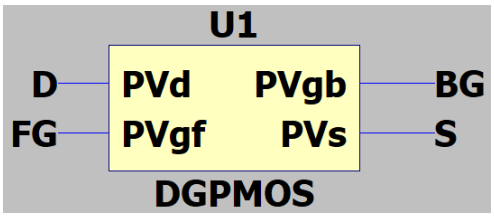

Figure 2: P-FinFET Sub circuit

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As working so far, all these parameters are drawn and the viable solution is that FinFET based technology is the technique to have all these characteristics in usage of transistor, power consumption and less in area and to implement the low power analyses we have different techniques to implement and consumption of power is analysed in both CMOS & FinFET technologies with the usage of low power technique and in normal condition. In order to analyse the power consumption in both CMOS & FinFET SRAM cell we are using the low power technique for reducing the power consumption in implementation of 6T and 8T SRAM cell. There are several techniques have been developed to reduce the power consumption of FinFET- based SRAMs.

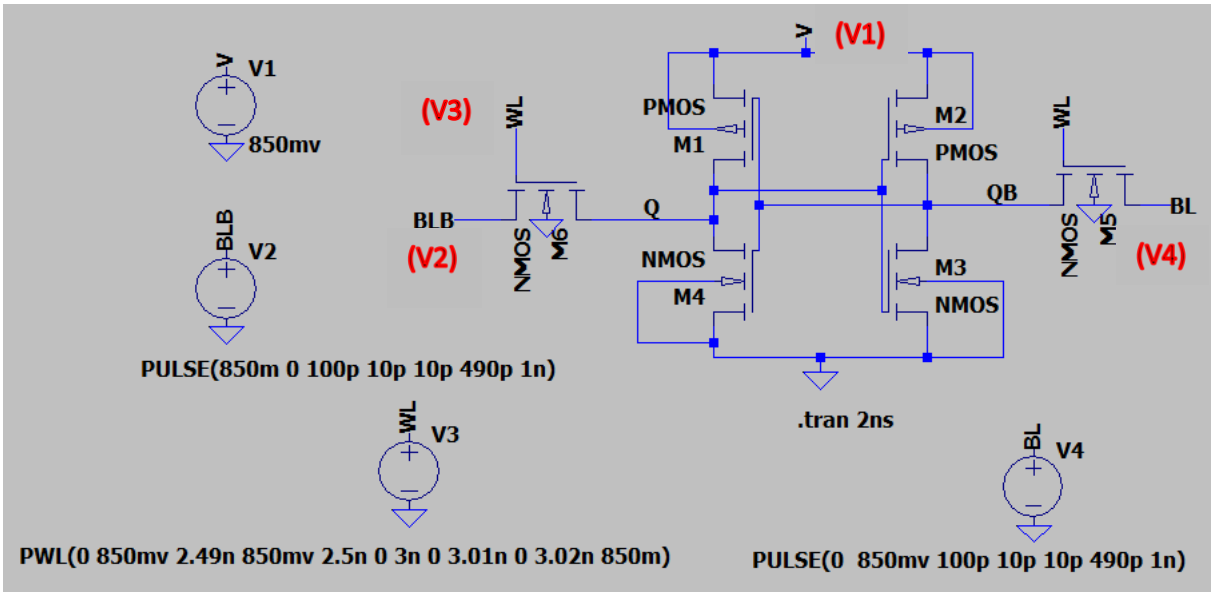

Figure 3: Implementation of 6T SRAM Cell using CMOS based technology

One of the primary techniques is Power Gating, which involves turning off the supply voltage to a part of the circuit when it is not required. This technique is used to reduce leakage power in idle periods of the SRAM cell, and we have chosen this technique for our project implementation for the better results in reducing the power consumption. Power gating technique is implemented for FinFET based 6T SRAM cell for reduction of power consumption.

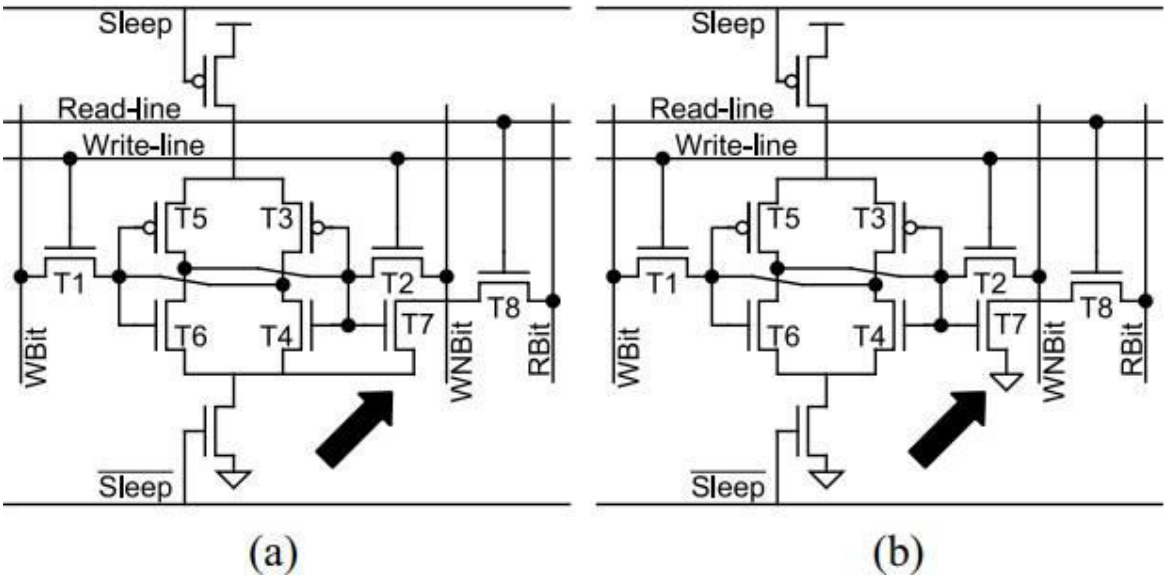

Figure 4: Conventional 8T SRAM Cell

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8T SRAM is implemented in both CMOS & FinFET based technologies along with power gating technique for reduction of power consumption.

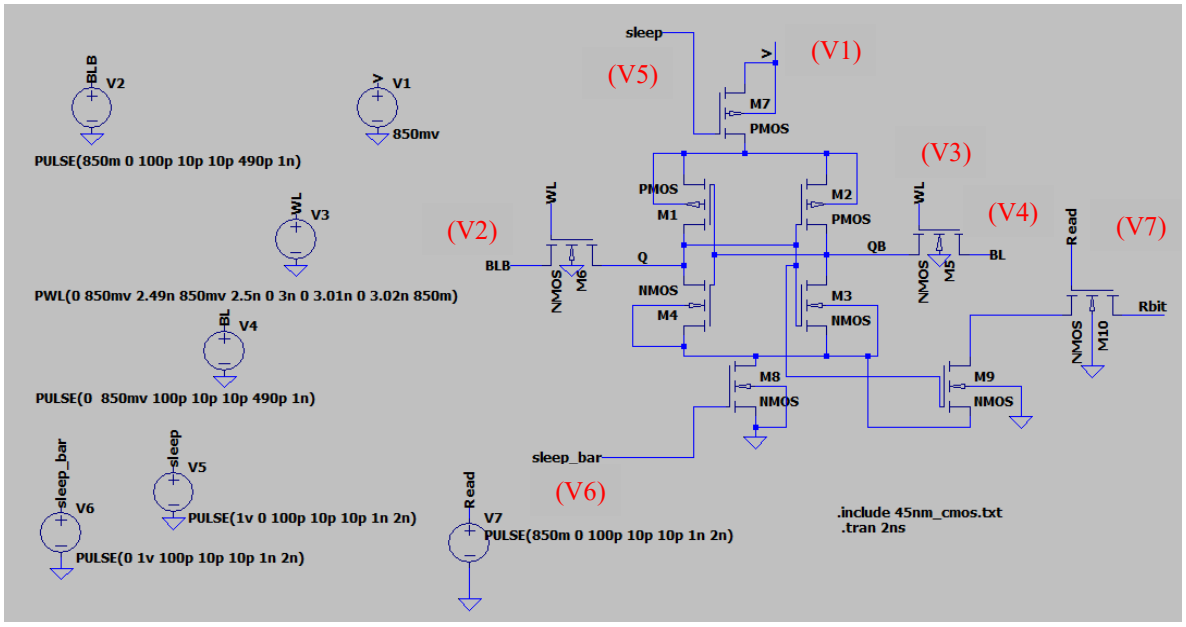

Figure 5: Implementation of Power Gating Technique for 8T SRAM Cell using CMOS

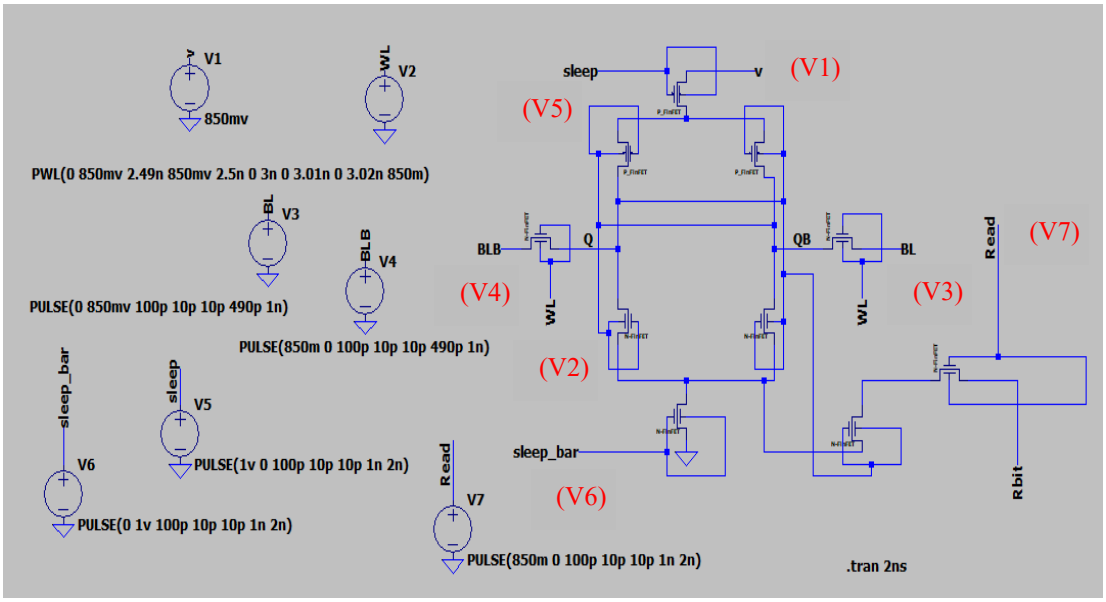

Figure 6: Implementation of Power Gating Technique for 8T SRAM Cell using FinFET

II. RESULTS AND DISCUSSIONS

Power calculations are drawn from the conventional 6T SRAM cells in both CMOS & FinFET technologies without using any of the power techniques for reduction of power consumption are shown in Table 6.1. For 8T SRAM cell for other representation (b) using power gating technique in both CMOS & FinFET technologies also calculated and shown in the table 2. Delay is calculated by taking V(q) vs V(qb) waveforms and overlap each other and find the delay differences for one complete cycle and take the average of both the peak values. For the 6T & 8T SRAM cells in both the CMOS and FinFET technologies, the average power and delay are measured. From the results, it can be found that the 6T SRAM implemented in FinFET maximally improve the power consumption by about 33.75% when compared

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with CMOS equivalent. Similarly, for 8T SRAM cell has a maximal improve of power consumption by about 12.278% when compared with CMOS equivalent circuit using power gating technique for reducing the power consumption for both the technologies. And it is observed that by using power gating technique it is consuming less power than the conventional SRAM cells for both 6T & 8T. The average power, individual power sources and delay are measured. From the results, it can be found that the 6T SRAM implemented in FinFET maximally improve the reduction of power consumption by about 33.75% when compared with CMOS equivalent. And it is observed that by using power gating technique it is consuming less power than the conventional SRAM cells for both 6T & 8T. Similarly, for 8T SRAM cell has a maximal improve of power consumption by about 12.278% when compared with CMOS equivalent circuit using power gating technique. And delay is improved by 5.71% for 6T SRAM cell and 2.781% for 8T SRAM cell when compared with CMOS by using power gating technique.

Table 1: Comparison power dissipation by using Power Gating and Conventional 6T SRAM Cell in both CMOS & FinFET technologies

6T SRAM				
Parameters	**With Power Gating Technique**		**Without Power Gating Technique**	
	CMOS	**FinFET**	**CMOS**	**FinFET**
BitLine_Bar	4.0203 **µW**	627.51 n**W**	1.131 n**W**	0.574 **µW**
Word Line	3.1629 **µW**	810.66 n**W**	0W	7.5661 **µW**
Bit line	3.1789 **µW**	626.33 n**W**	1.161 n**W**	6.418 **µW**
Hold	3.9621 **µW**	20.686 n**W**	-	-
Hold_bar	3.4765 **µW**	14.08 n**W**	-	-

Table 2: Comparison between CMOS & FinFET 8T SRAM using Power Gating Technique and without power gating Technique.

8T SRAM				
Parameters	**With Power Gating Technique**		**Without Power Gating Technique**	
	CMOS	**FinFET**	**CMOS**	**FinFET**
BitLine_Bar	4.0203 **µW**	722.76 n**W**	4.4550 **µW**	720.6 n**W**
Word Line	3.1629 **µW**	2.808 n**W**	347.95 nW	1.281 n**W**
Bit line	3.1789 **µW**	727.22 n**W**	3.5102 **µW**	677.1 n**W**
Hold	3.9621 **µW**	23.037 n**W**	60.372 n**W**	22.39 nW
Hold_bar	3.4765 **µW**	10.328 n**W**	365.77 nW	11.835 nW
Read	175.07 nW	-	224.61 nW	-

Table 3: Comparison between Average Power and Delay in both CMOS & FinFET using PowerGating Technique

Power Gating Technique				
	CMOS		**FinFET**	
Parameter	6T SRAM	8T SRAM	6T SRAM	8T SRAM
Power	-316.29nW	-337.26nW	-810.66pW	-2.808nW
Delay	5.4633ps	2.61371ps	4.3436ps	6.45661ps

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