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A Novel Fifteen-Level Inverter with Reduced Switches

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ABSTRACT- A new multilevel inverter with fewer power switches is proposed. This new multilevel inverter is based on reduced switch topology. This article will furnish reduced Total Harmonic Distortion (THD). This paper proposes a new switching concept with a smaller number of switches. This concept helps reduce wiring complexity compared to other tiered inverters. The proposed fifteen-level multi-level inverter with reduced switches is connected with a RL load. The proposed idea is confirmed by simulation.

KEYWORDS:15-level,Inverter, reduced switches, Modulation Techniques

1. INTRODUCTION

Today, multilevel inverters have become more common due to their voltage handling and efficiency. A multilevel inverter obtains the required power by using many independent DC voltage sources. The inverter voltage output waveform is obtained with an almost sinusoidal waveform where the number of DC sources increases using the switching frequency. It shows low switching losses and low voltage due to multiple DC sources. With low electromagnetic interference (EMI) power, it shows high efficiency and low switching losses, high voltage operation capability and more performance against multi-level inverters. The word multi-level starts with a three-level inverter. In power electronics applications, multilevel inverters are becoming more common because multilevel inverters can well meet the increased power and power quality requirements associated with reducing harmonic distortion and electromagnetic interference. In high switching frequency pulse width modulation (PWM), multilevel inverters have several advantages over the traditional two-level inverter. The most attractive features of a multi-level inverter are:

1) Output voltage can be produced with low distortion and dv/dt voltage.
2) The input current is taken with a small distortion.
3) The common mode voltage is very low.
4) It works at a low switching frequency.

Multilevel inverters are arranged with power-switching devices and capacitor voltage sources. It is suitable for high-voltage applications and voltage waveforms because they are able to measure the output voltage with better harmonics to achieve high voltages at the maximum values of the device. My-type multilevel inverters are diode-clamped, capacitor-clamped and cascaded H-bridge inverters. This requires fewer components in the capacitors and switches of each level and a less cascaded H-bridge inverter. This type consists of power converters connected in series and the power is easy to obtain. In multilevel inverters, the cascaded H-bridge provides a separate input voltage through a combination of capacitors and switches. It consists of H-bridge elements and each element can produce three different voltages such as zero, positive DC and negative DC. The main advantage of this multilevel inverter is that it requires fewer components compared to the other two types. The price and weight of the inverter are lower compared to the other two types. New switching methods can be created using soft switching. Conventional multiphase inverters use multilevel cascade inverters to eliminate THD and transformer harmonics, diode clamp inverters require clamp diodes, and flying capacitor inverters require flying capacitors. When a large number of isolated voltages are required to supply each element and compare the two types.This proposed topology has more advantages than the existing topologies because the number of switches and (THD) is reduced. Consequently, switching losses are also reduced, which increases production. The proposed multilevel inverter requires fewer switches and high efficiency with lower losses. Pulse width modulation (PWM) techniques are currently widely used due to their lower computational requirements, simplicity, and reliability.

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II. BLOCK DESCRIPTION

This multilevel inverter consists of three DC sources. Each source provides the required voltage to each switch. The controller circuit needs 12 volts, the image microcontroller needs 5 volts and the inverter circuit needs 24 volts. An inverter circuit converts current from direct current to alternating current using a rectifier. The rest of the driver circuit and the microcontroller use DC directly. The result is obtained.

The PWM switching frequency must be much higher than what would affect the load (power consuming device), ie. the waveform detected by the load must be as smooth as possible. The speed or frequency) at which the power supply must be switched can vary greatly depending on the load and application

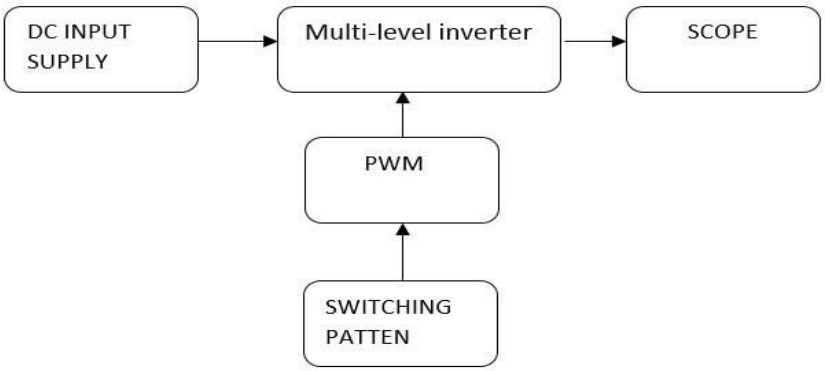

Fig1.Block diagram of proposed inverter

III. SIMULATION OF THE PROPOSED INVERTER WITH H-BRIDGE AND REDUCED SWITCHES

Cascaded H-Bridge 15-level inverter

The proposed topology is simulated in MATLAB. It consists of 28 front-end MOSFETs (S1-S28) connected to seven DC voltage sources of the same voltage and diodes connected to them as shown in the circuit. It also consists of 28 MOSFETs connected in an H-bridge design as shown in the circuit

The switching pulses are applied to the H-bridge circuit using a conventional sine pulse width modulation technique (to generate positive and negative cycles). The switching pulses of MOSFETs are given. These pulses are generated when the reference signal overlaps with the carrier signals. The pulses are produced with a delay given to each switch. Reference sine wave frequency 50 Hz.

The output voltage and current waveforms of the 15-level MLI show the FFT analysis, and the total harmonic distortion (THD) obtained is about 14.37% for the resistive load voltage. In this proposed system, we connected 15-level CHB in series to reduce or reduce the number of switches and minimize THD. The main objective of the proposed device is that the inverter produces a better quality output with less power loss compared to other conventional inverters with the same output quality. The general block diagram of the proposed inverter is shown in Figure 3, and the waveform of the proposed method is also shown.

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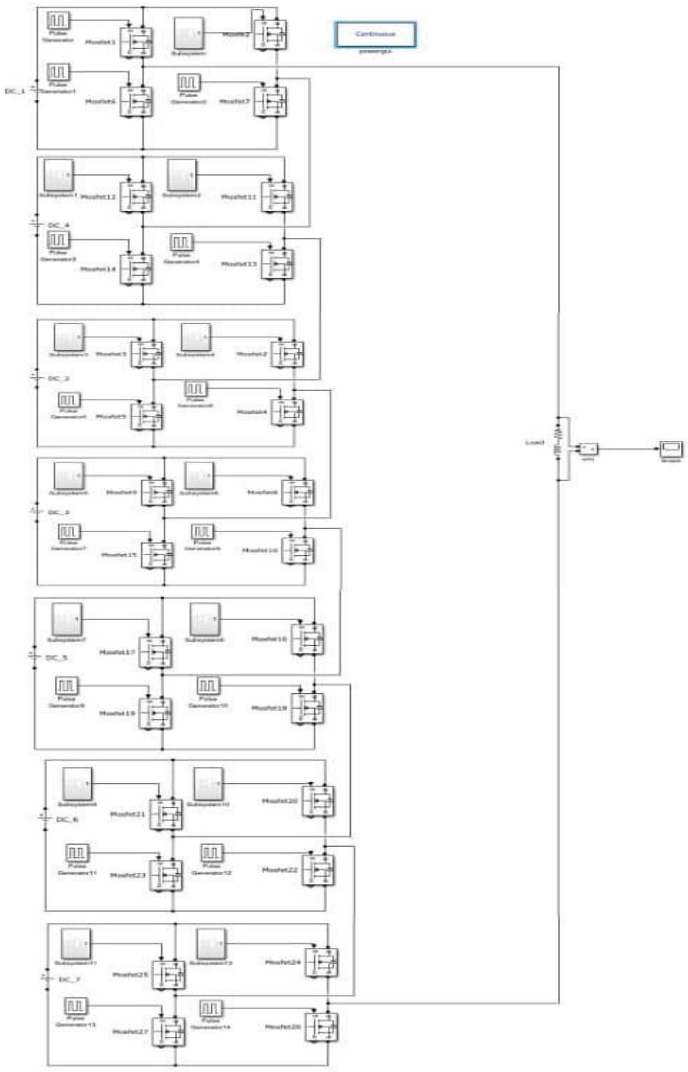

Fig2.Circuit diagram of CHB 15-level inverter with R load.

15-level inverter with reduced switches

The proposed topology is simulated in MATLAB. It consists of 9 front-end MOSFETs (S1-S9) connected to seven DC sources of the same voltage and diodes connected to them as shown in the circuit. It also consists of 9 MOSFETs connected in series as shown in figure 2 above

The switching pulses are applied to a 15-level circuit using the usual sine pulse width modulation technique (to generate positive and negative cycles). The switching pulses of MOSFETs are given. These pulses are generated when the reference signal overlaps with the carrier signals. The pulses are produced with a delay given to each switch. Reference sine wave frequency 50 Hz

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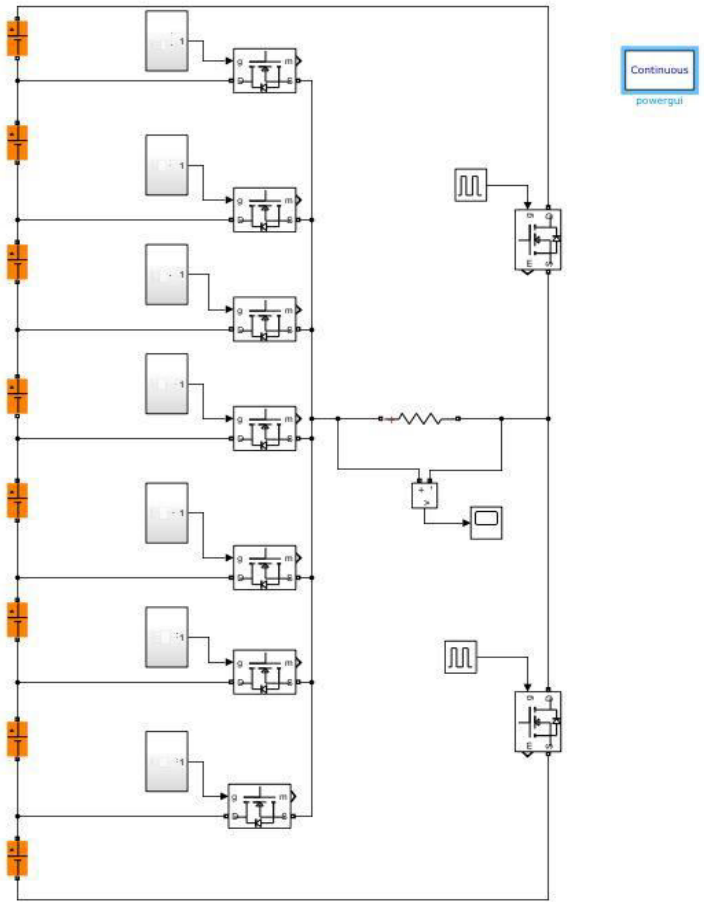

Fig3.Circuit diagram of CHB 15-level inverter with reduced switches with R load

The output voltage and current waveforms of the 15-level MLI show the FFT analysis, and the total harmonic distortion (THD) obtained is about 14.37% for the resistive load voltage. In this proposed system, we have a 15-level inverter connected in series with reduced switches to reduce or reduce the number of switches and minimize THD. The main objective of the proposed device is that the inverter produces a better quality output with less power loss compared to other conventional inverters with the same output quality. The general block diagram of the proposed inverter is shown in Figure 2, and the waveform of the proposed method is also shown

For example, consider the moment when the result is. The switch pulses given to the Hbridge IGBTs are controlled during normal operation. When some switches are ON, the other switches are OFF and vice versa.

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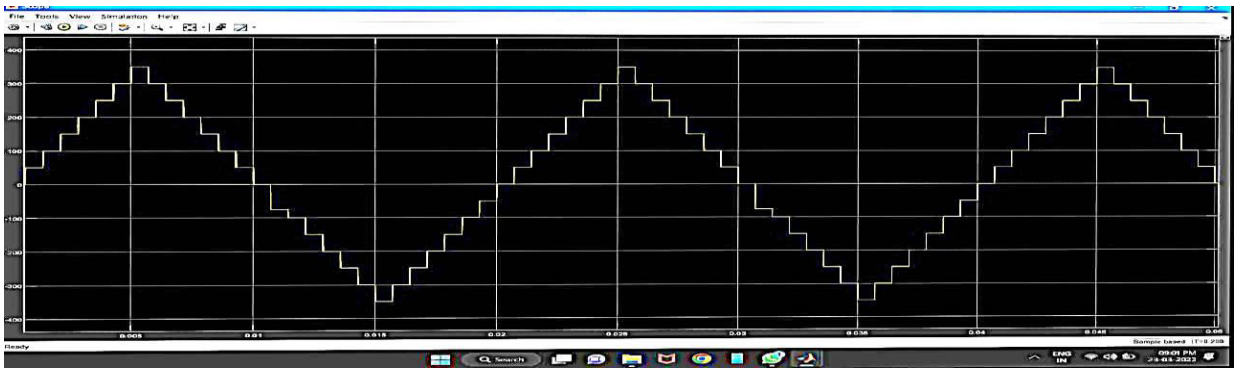
S7	S6	S5	S4	S3	S2	S1	S8	S9
0								
30	ON							ON
60		ON						ON
90			ON					ON
120				ON				ON
150					ON			ON
180						ON		ON
210							ON	ON
180						ON		ON
150					ON			ON
120				ON				ON
90			ON					ON
60		ON						ON
30	ON							ON
0								
-30							ON	
-60						ON		
-90					ON			
-120				ON				
-150			ON					
-180		ON						
-210	ON							
-180		ON						
-150			ON					
-120				ON				
-90					ON			
-60						ON		
-30							ON	

Table 1 Switching table for proposed reduced switch inverter

Initially, all switches are off. In this model, the voltage is 15 degrees. i.e. 7 levels for each positive and negative half cycle and zero level.The bridge voltages are added based on the switching functions given by the pulse generators.Positive half-period switches are used 1,2,3,5,6,7,8,9 and negative half-period switches are used 1,2,3,4,6,7,8,9.

The pulses of the cascade element are supplied directly through the pulse generator and the pulses to the Mosfet as input pulses from the output of the PWM generation circuit. The pulse generator block produces square

Fig 4. Scope output of 15-level inverter with reduced switches



wave pulses at regular intervals. This block has pulse width and phase delay parameters. The output of the block can be generated in timed or sampled mode, which is determined by the pulse type parameter. The switching pulses are applied to the 15 level circuit using a conventional sine pulse width modulation technique (to generate positive and negative cycles). The switching pulses of MOSFETs are given. These pulses are generated when the reference signal overlaps with the carrier signals. The pulses are produced with a delay given to each switch. Reference sine wave frequency 50 Hz. .

$$Pulse\ width = \frac{width\ of\ the\ pulse}{full\ cycle} \times 100 \quad ; \qquad Phase\ delay = \frac{0.02}{full\ cycle} \times pulse\ level \quad \therefore \frac{1}{f} = 0.02$$

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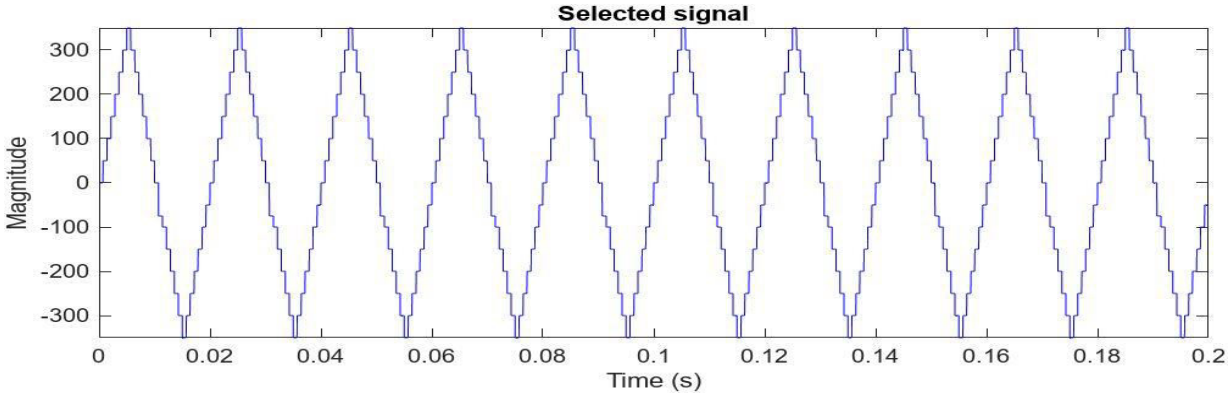

Fig. 5 .Simulation output of 15-level inverter

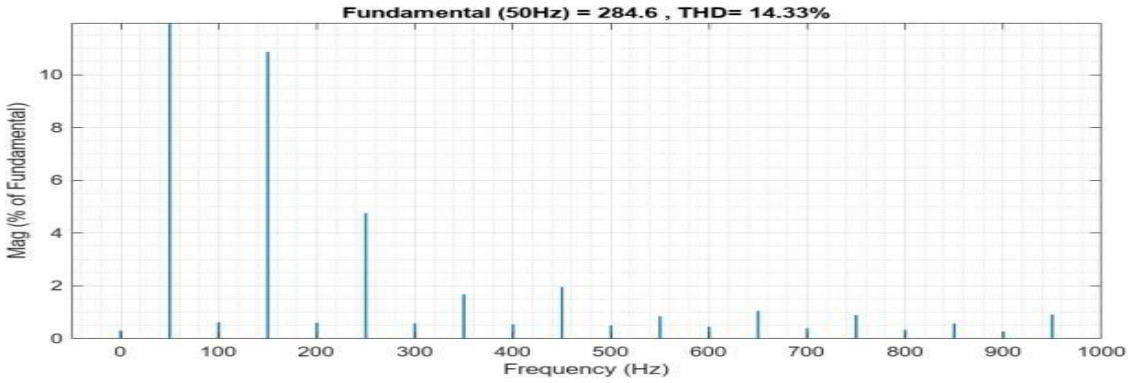

Fig 6. THD output with R load of 15-level

Total Harmonic Distortion (THD) is a measure of harmonic contamination in a power system, and variations in both DC voltage and inverter switching angles have been found to affect the THD of the inverter output voltage. DC sources in cascaded multilevel symmetrical inverters are ideally equal and constant.

Advantages:

1) It provides a simple interface for grid integration of renewable energy resources.
2) Multi-level output waveform improves power quality (low THD output).
3) There is very little distortion in the input stream

Disadvantages:

1) Complex circuit.
2) Cost increases with an increase in switches.
3) Due to the many switches in multilevel inverters, multiple gate pulses must be generated, which again requires the use of advanced PWM- based digital signal processors

Applications:

1) UPS.
2) High voltage DC transmission.
3) Variable Frequency Drives

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IV. CONCLUSION

The outcomes for the proposed framework are clarified within the underneath:The proposed MLI uses only 9 switches to generate 15 output levels. The results of the simulation revealed that the THD of the output voltage and current of the proposed system are low and compared to the existing one.The inverter expands by increasing the level with a minimum number of switches, the total cost decreases and the inverter produces a high output voltage. This article proposes a fifteen-level multilevel inverter with a minimum number of switches. This produces a sinusoidal waveform and high voltage. This improves the performance of the series multilevel inverter. This type of switching loss is reduced and so is the total harmonic distortion

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